501.36269CC5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Y. Tanabe, et al.

Application No. Rule 53(b) of No. 10/355,301

Filed: April 12, 2004

For: FABRICATION PROCESS OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Expected Examiner: G. Peralta

Expected Group: 2814

CLAIM FOR PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 12, 2004

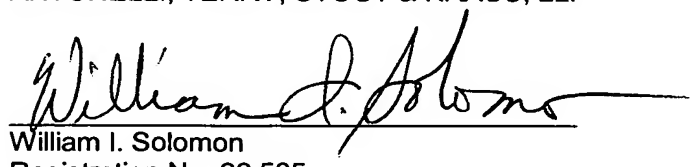
Sir:

Pursuant to the provisions of 35 USC §119 and 37 CFR § 1.55, Applicants hereby claim the right of priority based on Japanese Patent Application No. 11-142315, filed May 30, 1997.

A certified copy of the above-referred-to Japanese Patent Application was submitted on May 29, 1998, in prior application No. 09/086,568, filed May 29, 1998.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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